IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket: CY-0006

In re application of: **JIN et al.**

Serial No.: **09/405,945** Group No.: **1765**

Filed: **September 27, 1999** Examiner: **Umez Eronini, L.**

Assistant Commissioner for Patents
Washington, D.C. 20231
Attention: **Board of Patent Appeals and Interferences**

APPELLANT'S BRIEF

Timing of Appeal Brief and Fees Required Pursuant to 37 C.F.R. 1.192(a)(b)

This brief is in furtherance of the Notice of Appeal, filed in this case on November 16, 2001.

The fees required under 37 C.F.R. 1.17(f), and any fees for a petition for extension of time for filing this brief are dealt with in the accompanying Transmittal of Appeal Brief.

Certificate of Mailing/Transmission (37 C.F.R. 1.8(a))

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Appeal Brief Items Pursuant to 37 C.F.R. 1.192(c)

This brief contains the following items under the headings, and in the order set forth below.

1. Real Party in Interest
2. Related Appeals and Interferences
3. Status of Claims
4. Status of Amendments
5. Summary of Invention
6. Issues
7. Grouping of Claims
8. Argument
9. Appendix

1. Real Party in Interest

The patent application on appeal is owned, by assignment, by Cypress Semiconductor Corporation, a Delaware Corporation, having offices at 3901 North First Street, San Jose, CA 95134.

2. Related Appeals and Interferences

There are no other appeals or interferences related to, or that may be affected by a decision of the Board of Patent Appeals and Interferences (the Board) on this appeal.

3. Status of Claims

The status of all claims is set forth below.

Claims cancelled: Claims 15 and 20.

Claims allowed: None.

Claims rejected: Claims 1-14 and 16-19.

The claims on appeal are claims 1-14 and 16-19.

4. Status of Amendments

No amendments were submitted after the final rejection.

5. Summary of Invention

The invention of claim 1 is directed toward a method of forming a contact hole through a first insulating layer (e.g., FIG. 1, item **106**, FIG. 2C and the Specification, page 13, lines 6-14 and page 13, line 21 to page 14, line 3; FIG. 3, item **306**, FIG. 4C and the Specification, page 16, lines 16-21; FIG. 5, item **522**, FIG. 6K and the Specification, page 24, line 4 to page 25, line 3). The etched contact hole is self-aligned with respect to a transistor gate (e.g., the Specification, page 4, lines 8-10, page 24, Lines 3-4). The transistor gate has a gate length of less than 0.2 microns (e.g., the Specification, page 27, Table 1, where a Poly CD Final value is 0.160, and page 9, lines 15-17). The contact hole is formed without forming an etch stop liner (e.g., FIGS.

2C and 2D, and the Specification, page 12, lines 2-5, page 13, lines 15 to 20; page 14, lines 1-3; FIGS. 4B and 4C, and the Specification, page 15, lines 17 to 22, page 16, lines 23-24; FIG. 6K and the Specification, page 20, line 2, page 26, lines 9-10).

The invention of claim 3 includes the various steps described for claim 1, but adds that forming a contact hole includes reactive plasma etching (e.g., the Specification, page 13, line 13; page 24, line 5 to page 25, line 5). Further, such etching is through a first insulating layer comprising silicon dioxide. The silicon dioxide has a phosphorous dopant concentration that is greater than 5% by weight (e.g., the Specification, page 12, lines 5-11).

The invention of claim 12 is a method that includes etching a contact hole through a first insulating layer (e.g., FIG. 1, item **106**, FIG. 2C and the Specification, page 13, lines 6-14 and page 13, line 21 to page 14, line 3; FIG. 3, item **306**, FIG. 4C and the Specification, page 16, lines 16-21; FIG. 5, item **522**, FIG. 6K and the Specification, page 24, line 4 to page 25, line 3). The first insulating layer comprises doped silicon dioxide (e.g., e.g., the Specification, page 12, lines 5-11). The contact hole is self-aligned with respect to a conductive structure (e.g., the Specification, page 4, lines 8-10, page 24, Lines 3-4). The conductive structure is formed over a substrate and includes insulating sidewalls (e.g., FIGS. 2A to 2D, items **204** and **206**, and the Specification, page 11, lines 16-17; FIGS. 4A to 4D, items **402**-1 and **404**-1, and the Specification, page 14, line 24 to page 15, line 1; FIGS. 6D to 6K, items **618**-1 and **618**-2, and the Specification, page 19, line 24 to page 20, line 1). Etching is performed with particular etch selectivity parameters. The etch selectivity between the first insulating layer and the sidewall is greater than ten to one (e.g., the Specification, page 25, lines 7-8). The etch selectivity between the first insulating layer and substrate is greater than one hundred to one (e.g., the Specification, page 25, lines 18-20).

The invention of claim 18 is a method that includes forming a hard mask comprising substantially undoped silicate glass (e.g., FIGS. 6I to 6K, and the Specification, page 22, lines 8-9, and page 23, lines 2-7). The hard mask is formed over an insulating layer comprising doped silicon dioxide (e.g., FIG. 6G, the Specification, page 22, lines 6-7). The hard mask has

openings over a contact hole location (e.g., the Specification, page 23, lines 11-12). A contact hole is formed at the contact hole location through the first insulating layer (e.g., FIG. 1, item **106**, FIG. 2C and the Specification, page 13, lines 6-14 and page 13, line 21 to page 14, line 3; FIG. 3, item **306**, FIG. 4C and the Specification, page 16, lines 16-21; FIG. 5, item **522**, FIG. 6K and the Specification, page 24, line 4 to page 25, line 3). The contact hole is formed between conducting structures that are separated from one another by less than 0.4 microns (e.g., the Specification, page 27, Table 1, where a Poly Pitch has a value of 0.460 microns and a Poly CD Final value is 0.160 microns, thus a separation distance is 0.460-0.160 = 0.300 microns). The conducting structures have sidewalls (e.g., FIGS. 2A to 2D, items **204** and **206**, and the Specification, page 11, lines 16-17; FIGS. 4A to 4D, items **402**-1 and **404**-1, and the Specification, page 14, line 24 to page 15, line 1; FIGS. 6D to 6K, items **618**-1 and **618**-2, and the Specification, page 19, line 24 to page 20, line 1). The contact hole is formed without forming a protective liner over the conducting structures (e.g., FIGS. 2C and 2D, and the Specification, page 12, lines 2-5, page 13, lines 15 to 20; page 14, lines 1-3; FIGS. 4B and 4C, and the Specification, page 15, lines 17 to 22, page 16, lines 23-24; FIG. 6K and the Specification, page 20, line 2, page 26, lines 9-10).

6. Issues

The issues presented for review are set forth below.

Issue 1 - Whether claims 1, 2 and 7-11 are patentable over *Hsue* (U.S. Patent No. 5,738,654) in view of *Chang et al.* (U.S. Patent No. 5,893,740).

Issue 2 - Whether claims 3-6 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.* (U.S. Patent No. 5,468,342).

Issue 3 - Whether claims 12-17 are patentable over *Hsue* in view of *Chang et al.*

Issue 4 - Whether claims 18 and 19 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Avanzino et al.* (U.S. Patent No. 5,776,834).

7. Grouping of Claims

Claims 1, 2 and 7-11 stand or fall together.

Claims 3-6 stand or fall together.

Claims 12-17 stand or fall together.

Claims 18 and 19 stand or fall together.

8. Argument

8(i) Rejections Under 35 U.S.C. §112, First Paragraph

No claims were rejected on these grounds.

8(ii) Rejections Under 35 U.S.C. §112, Second Paragraph

No claims were rejected on these grounds.

8(iii) Rejections Under 35 U.S.C. §102

No claims were rejected on these grounds.

8(iv) Rejections Under 35 U.S.C. §103

The following arguments explain why the claim groups indicated in Section 7 are believed to be separately patentable.

Issue 1 - Whether claims 1, 2 and 7-11 are patentable over *Hsue* in view of *Chang et al.*

Independent claim 1 recites a method that includes forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate. The transistor gate has a gate length of less than 0.2 microns. Further, the contact hole is formed without a contact hole etch stop liner.

In rejecting claim 1, the Office Action admits that that while *Hsue* shows a self-aligned contact etch, *Hsue* does not show a transistor with a gate length of less than 0.2 microns.[1] To show a transistor with a gate length of less than 0.2 microns, *Hsue* is modified by *Chang et al.*, which teaches a short channel field effect transistor with a gate length of 0.1 microns.

The motivation for the combination relied upon by the rejection was stated in the Final Office Action.

> *Hsue*'s and *Chang*'s reference is related to the manufacturing of field effect transistors. Hence it would be obvious to modify *Hsue*'s gate structure, which is the same as the transistor of the claimed invention, by using a transistor with a gate length of less than 0.2 microns as taught by *Chang* fro the purpose of increasing the speed of the transistor.[2]

A <u>prima</u> <u>facie</u> case of obviousness requires there must be some suggestion or motivation to combine reference teachings. However, if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or

[1] See the Final Office Action dated 08/16/01 (Paper 7), Page 2, last full paragraph.

motivation to make the proposed modification.[3] Because the combination of *Hsue* in view of *Chang et al.* would render the reference *Hsue* unsatisfactory for its intended purpose, the motivation relied upon in rejecting claim 1 does not exist.

The reference *Hsue* teaches a self-aligned contact process. As shown in *Hsue*, a self-aligned contact is a contact formed adjacent to a conductive structure. The contact remains electrically isolated from the contact by insulating sidewalls and a top insulating layer.[4] This was also noted in Appellants' Specification.[5]

Chang et al. is not compatible with the *Hsue* process. *Chang et al.* teaches a short channel field effect transistor that does not include an insulating or dielectric layer formed on the top of the gate.[6] Incorporating the transistor of *Chang et al.* into the *Hsue* process would defeat the SAC process, as no structure would exist to prevent the gate from being exposed when the contact hole is etched. That is, there is no structure over the top of the gate that would insulate the conductive gate from a subsequently formed conductive contact.

If it is argued that only a gate of *Chang et al.* need be incorporated into the teachings of *Hsue*, such a modification also renders the resulting device unsatisfactory. Unlike *Hsue*, which appears to be directed to relatively large device sizes[7], transistors the size of *Chang et al.* need to have short channel effects suppressed.[8] To address short channel effects, *Chang et al.* teaches particular features, including particular ion implantation doses to form short channel source and drain regions, as well as a tilt ion implantation step that necessarily relies on a silicide layer on the top of the gate, a silicide layer on the substrate, as well as a particular sidewall on the gate.[9] However, as noted above, such structures are not suitable for a self-aligned contact process.

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[2] See *infra*, Page 7, Lines 5-9.

[3] In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).

[4] See *Hsue*, FIG. 1F, where a conductive contact 28 is isolated from gates 12, by insulating sidewalls 18 and top insulating layer 14.

[5] See the Specification, page 4, lines 7-10.

[6] See *Chang et al.*, FIGS. 1(b) and 3(b), which show a silicide layer formed on the top of the gate electrode. No dielectric layer is formed on the gate.

[7] See Applicants' Response to Office Action, dated June 14, 2001, page 2, line 20 to page 3, line 2.

[8] See *Chang et al.*, Col. 1, Lines 10-15.

[9] See *Chang et al.*, Col. 3, Lines 49-54 and FIGS. 1(c) and 3(c), which note that silicide layers 17 on a gate and substrate serve as a mask

Thus, a combination that incorporates only a gate of *Chang et al.* into the process of *Hsue* needs some additional teaching, not shown in any of the cited references, to ensure that the resulting device does not suffer from short channel effects. The techniques to address short channel effects set forth in *Chang et al.* are not compatible with the *Hsue* process.

To summarize, the reference *Hsue* is directed toward devices having gate lengths that are large relative to Appellants' claimed limit. *Chang et al.* is directed to relatively small devices that suffer from short channel effects, and hence require features that are not compatible with the process of *Hsue*.

Accordingly, because a prima facie case of obviousness has not been established for the rejection of claim 1, Appellant seeks reversal of the rejection of claim 1.

Issue 2 - Whether claims 3-6 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.*

The invention of claim 3, includes the limitation of claim 1, but further adds that forming the contact hole includes reactive plasma etching through the first insulating layer, where the first insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

The rejection of claim 3 admits that the references do not show a phosphorous dopant concentration greater than 5% by weight.[10] To show Appellants' particular concentration limitation, the rejection appears to argue that the range would be obvious through routine experimentation.[11]

The obviousness of ranges rationale relied upon is believed to be in error for a number of reasons. First, the obviousness of ranges rationale has been improperly applied. Second, Appellants' un-rebutted background art teaches away from the claimed range. Finally, the prior art does not recognize the concentration of phosphorous as a result effective variable.

for a tilt (LATI) implant. As shown in FIG. 1(c), impurities are implanted through a sidewall.

[10] See the Final Office Action, dated 8/16/01, page 8, lines 10-11.

[11] See *infra*, page 8, lines 12-17.

It is well established that in cases where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum workable ranges by routine experimentation.[12] However, none of the prior art discloses any concentration conditions as recited in claim 3. Appellants' admit that the reference *Nulty et al.* discloses silicon dioxide that may be doped with boron, phosphorous, or both.[13] However, no percentage is disclosed. Thus, working from the cited combination of references, one skilled in the art would have no particular phosphorous concentration value to optimize.

Thus, the rationale relied upon has no basis in the prior art, and hence is improper. Thus, a case of prima facie obviousness has not been made.

The obviousness of ranges rationale relied upon is further believed to be in error as Appellants' background art teaches away from the cited range. No other evidence has been presented to rebut this evidence. As noted above, the cited reference *Nulty et al.* discloses phosphorous doped silicon dioxide. However, Appellants' Specification explicitly indicates that high phosphorous concentrations (e.g., the range recited in Appellants' claim 3) have deleterious effects.[14] No evidence has been offered to rebut this teaching.

Thus, Appellants' claimed range would not be obvious by routine experimentation as conventional approaches teach away from such ranges.

Finally, a determination that a variable may be characterized by routine experimentation requires that the variable be recognized as a result effective variable. That is, a variable which achieves a recognized result.[15] None of the cited art indicates that the concentration of phosphorous achieves a recognized result. *Hsue* only shows examples of undoped silicon dioxide (i.e., no phosphorous).[16] *Chang et al.* is entirely unrelated to contact formation and so provides no teachings regarding insulating layers. *Nulty et al.* describes a silicon dioxide doped with phosphorous, but phosphorous is not noted as a result effective variable.[17] Finally, as noted

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[12] In re Aller, 105 USPQ 233, 235 (CCPA 1976).
[13] See *Nulty et al.*, Col. 1, Lines 17-25.
[14] See the Specification, page 6, line 21 to page 7, line 6, page 7, lines 12-18.
[15] In re Antonie, 195 USPQ 6 (CCPA 1977).
[16] See *Hsue*, Col. 2, Lines 3-5 and Col. 4, Lines 19-22, which describe silicon dioxide layers **21** and **46**, with no indication of doping.
[17] See *Nulty et al.*, Col. 1, Lines 17-25.

above, Appellants' background art indicates that increasing phosphorous concentration in a BPSG film is essentially the opposite of a result effective variable, as deleterious effects may result.

In summary, the range of phosphorous concentration recited in claim 3 would not be a variable that would be obviously optimized as 1) no reference indicates initial conditions for optimization, 2) Appellants' un-rebutted background art teaches away from the claimed range, and 3) no reference teaches that phosphorous is a result effective variable.

For all of these reasons, Appellants' respectfully request that the rejection of claims 3-6 be reversed.

Issue 3 - Whether claims 12-17 are patentable over *Hsue* in view of *Chang et al.*

The method of independent claim 12 includes etching a contact hole through a first insulating layer comprising doped silicon dioxide. The contact hole is self-aligned with respect to a conductive structure that is formed over a substrate. The etching has two particular etch selectivity limitations. The etch selectivity between the first insulating layer and the sidewall is greater than ten to one. The etch selectivity between the first insulating layer and the substrate is greater than one hundred to one.

The rejection of claim 12 admits that the cited references do not show Appellants' claimed etch selectivities.[18] To show the etch selectivity limitations, the rejection relies on the rationale set forth below.

> ...using the etching methods, oxide insulating layer and insulating sidewall materials of *Hsue*, <u>which are the same</u> as those of the claimed invention would inherently result in obtaining the same etch selectivities as claimed in the present invention... (emphasis added) [19]

[18] See the Final Office Action, dated 8/16/01 (Paper No. 7), page 8, last 2 lines to page 9, lines 1-2.
[19] See *infra*, page 9, lines 2-5.

The facts relied upon for the rejection are incorrect. *Hsue* does not teach the same materials as Appellants' claim 12. Claim 12 clearly recites doped silicon dioxide. *Hsue* does not show a first insulating layer of doped silicon dioxide.[20] Thus, the cited reference does not show the same materials as Appellants' claimed invention, and so cannot inherently obtain the same etch selectivities, as argued.

Because the etch selectivities recited in claim 12 are not inherent in the method of *Hsue*, no prima facie ground of obviousness exists, and the rejection of claims 12-17 should be reversed.

Issue 4 - Whether claims 18 and 19 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Avanzino et al.*

The method of independent claim 18 includes forming a hard mask comprising substantially undoped silicate glass. The hard mask is formed over an insulating layer comprising doped silicon dioxide. The hard mask also includes openings over contact hole locations.

The method further includes forming a contact hole at the contact hole location through the insulating layer. The contact hole is formed between conducting structures separated from one another by less than 0.4 microns. The conducting structures have sidewalls. Finally, the contact hole is formed without forming a protective liner over the conducting structures.

As is well established, a prima facie case of obviousness requires that all claim limitations must be taught or suggested by the prior art.[21]

The rejection of claim 18 admits that the references fail to show a hard mask comprising undoped silicate glass over an insulating layer comprising doped silicon dioxide.[22] To show the hard etch mask of claim 18, the rejection relies on the rationale set forth below.

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[20] See *Hsue*, Col. 2, Lines 3-5 and Col. 4, Lines 19-22, which describe silicon dioxide layers **21** and **46**, with no indication of doping.
[21] In re Royka, 180 USPQ 580 (CCPA 1974).
[22] See the Final Office Action, dated 8/16/01, (Paper No. 7), page 5, lines 8-11.

> ...it would have been obvious to one having ordinary skill in the art... to use conventional materials such as undoped silicon dioxide and doped silicon dioxide respectively, as a hard etch mask and first insulating layer for the purpose of forming a contact region in a semiconductor substrate.[23]

Appellants' note that this reasoning is not based on any cited reference. As admitted, the reference relied upon are entirely silent as to hard masks. Accordingly, such a teaching cannot be inherent or an obvious optimization of a disclosed condition.

In fact, the reasoning re-constructs the combination of elements recited in Appellants' claim 18 with no suggestion or motivation other than "for the purpose of forming a contact region in a semiconductor substrate." This appears to be the very definition of hindsight.

In summary, because claim 18 includes limitations not shown in any of the cited references, and the rejection relies on improper hindsight to teach such limitations, a prima facie case of obviousness does not exist. Accordingly, the reversal of this ground for rejection is respectfully requested.

Conclusion.

For the various reasons set forth above, Appellants' respectfully contends that a prima facie case was never established for the claims at issue. Accordingly, a reversal of all claim rejections is respectfully requested.

Respectfully Submitted,
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February 19, 2002 — Date

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[23] See *infra*, page 5, lines 12-16.

APPENDIX A

CLAIMS INVOLVED IN THE APPEAL

1. A method, comprising:

forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate having a gate length less than 0.2 microns without forming a contact hole etch stop liner.

2. The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising non-densified doped silicon dioxide.

3. The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

4. The method of claim 3, wherein:

the reactive plasma etching includes introducing CHF_3 and $C_2H_2F_4$ into an etch chamber.

5. The method of claim 4, wherein:

the flow rate of CHF_3 is less than ten times the flow rate of $C_2H_2F_4$.

6. The method of claim 5, wherein:

the flow rate of CHF_3 is in the general range of 3-15 standard centimeter cubed per minute (sccm); and

the flow rate of $C_2H_2F_4$ is in the general range of 10-100 sccm.

7. The method of claim 3, wherein:

the reactive plasma etching includes exciting a plasma with a radio frequency power source that supplies power in the general range of 100 to 1000 Watts.

8. The method of claim 3, wherein:

the reactive plasma etching includes an etch time in the general range of 80 to 200 seconds.

9. The method of claim 3, wherein:

the contact hole is formed on a target object that is biased to an absolute value potential in the general range of 100 to 1500 Volts.

10. The method of claim 3, wherein:

the reactive plasma etching pressure is in the general range of 20-100 milliTorrs.

11. The method of claim 3, wherein:

the reactive plasma etching temperature is in the general range of 0-35 °C.

12. A method, comprising:

etching a contact hole, through a first insulating layer comprising doped silicon dioxide, that is self-aligned with respect to a conductive structure that is formed over a substrate and includes insulating sidewalls with an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

13. The method of claim 12, wherein:

the insulating sidewalls comprise silicon nitride.

14. The method of claim 12, further including:

forming the first insulating layer comprising a high density plasma silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

16. The method of claim 12, further including:

forming a hard etch mask comprising an insulating material over the first insulating layer; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one.

17. The method of claim 16, wherein:

the hard etch mask comprises silicon dioxide; and

the first insulating layer comprises phosphorous doped silicon dioxide.

18. A method, comprising:

forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide, the hard mask having openings over a contact hole location; and

forming a contact hole at the contact hole location through the insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures.

19. The method of claim 18, wherein:

the insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight; and

the sidewalls comprise silicon nitride.